Mitesh Jain

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Summary

Over 8 years of industry experience in functional (formal and simulation-based) verification, performance and power modeling of microprocessors

Education

Northeastern University, Boston 2010-present
PhD Computer Science
`Thesis Proposal:` A refinement-based approach to reasoning about optimized reactive systems.
`Advisor:` Pete Manolios
`Expected Graduation:` Summer 2017

Indian Institute of Technology, Kanpur, India 1998-2002
B.Tech Electrical Engineering

Publications

A Refinement-based Approach to Testing of Hardware and Low-level Software Designs DAC 2016
Mitesh Jain and Panagiotis Manolios
Design Automation Conference, 2016

Proving Skipping Refinement with ACL2s ACL2 2015
Mitesh Jain and Panagiotis Manolios
International Workshop on the ACL2 Theorem Prover and its Application

Skipping Refinement CAV 2015
Mitesh Jain and Panagiotis Manolios
Computer Aided Verification

Practical Formal Verification of Domain-Specific Language Applications NFM 2015
Greg Eakman, Howard Reubenstein, Mitesh Jain,
Panagiotis Manolios, and Tom Hawkins
NASA Formal Method Symposium

Verification of Sequential Circuits by Tests-As-Proofs Paradigm arXiv 2013
Eugene Goldberg, Mitesh Jain, Panagiotis Manolios
E-print, arXiv

Skipping Refinement: Poster FMCAD 2013
Mitesh Jain and Panagiotis Manolios
Student Forum, Formal Methods in Computer Aided Design

Industrial Experience

Advanced Micro Devices, India 2004 - 2010
Senior Design Engineer

I worked on both core and uncore components of AMD's Greyhound and Bobcat architecture. I was responsible for devising several new microarchitectural features, developing performance and power models, and testing and verification.

Nulife Semiconductors Inc., India 2003-2004
Design Engineer

This start-up developed the lowest power digital hearing aid with a programmable processor. I was among the first five employees and was involved in several aspects of the product design ranging from defining the instruction set for the processor, its RTL implementation, and synthesis, and a compile-time power-estimation tool.

National Instruments, India 2002-2003
Software Engineer

I worked on developing device drivers for data-acquisition cards.

Internship

Mathworks, Natick, MA Summer, 2016
Evaluate state-of-the-art model-checkers and SMT solvers for automatic test-case generation and proving functional correctness of infinite-state systems.

Advanced Micro Devices, Boxborough, MA Summer, 2012
Analyzed server benchmarks for program behavior characterization and design predictors for front-end performance enhancements.

Languages

ACL2, C, Verilog, Python, Ocaml

Awards and Recognitions

Student Scholarship, CAV	2015
NSF Scholarship for SRI Summer School	2014
Student Travel Grant, FMCAD	2013
University Excellence Fellowship at Northeastern University	2010-2015
Vice President SpotLight Award at AMD	2009

Teaching Assistance

College of Computer Science, Northeastern University

Fall 2010, Spring 2011, Fall 2011, Spring 2013, Spring 2016