College of Computer Science
Northeastern University
COM 1722: Freshman Honors Seminar

Winter 2003
Handout 4
14 January 2003

Homework 2 (due Jan 28)

1. Multiplexers and Demultiplexers

(a) Using the gates that you have designed so far, design a 4-way 1-bit demultiplexer.

(b) A *k-way b-bit multiplexer* is one in which each of the k inputs is a group of b bits rather than a single bit, and the output is a group of b bits. There are also $\log_2 k$ control bits (assume that k is a power of 2), and these control bits are used to select one of the k groups of b bits rather than a single bit. Explain how to contruct a k-way b-bit multiplexer. You do not need to draw any circuits. Start with the setting $k = 4$, $b = 2$, and then generalize.

2. Registers

(a) Using a combination of clocked and unclocked NOT gates, show how to design a 4-bit register. The register should accept a 4-bit value on its 4 inputs before a clock pulse, and it should put that value on its 4 outputs.

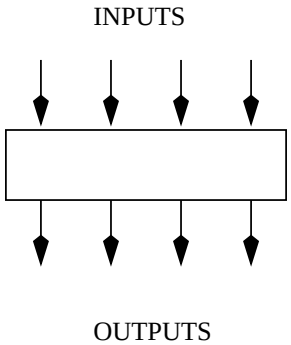

Figure 1: A 4-bit register.

(b) The register from the previous problem only holds values for one clock cycle. It is much more helpful if we could design the register so as to hold the values for an extended period of time. Extend the register circuit from above so that it accepts an extra input S (for Set). If S is 1, then the new circuit should behave exactly as above when the clock pulses. However, if S is 0 when the clock pulses, then the register should ignore its inputs, keeping the same outputs as before the clock pulse.