- midterm review
- I/O and DMA
- disks, block devices, RAID

I/O and DMA

This is for a toy computer

\( F_{xxx} \rightarrow \) framebuffer

\( EFFF \rightarrow \) RAM

\( 0000 \)
for modern CPU

~ 3 GHz

CPU  →  L1  1 cycle  →  L2  /  L3  →  RAM  →  PCI

300 cycles

DOR 2/3

We push data, don't pull it
so we use DMA for that

memory  /  I/O registers

CPU

→ prepare DMA desc
  cmd
  pty

→ put & desc
  in circular buf

→ update 'head' register

→ read status
  done
Device

read & desc

[read desc]

does something

[write data]

set status

← interrupt

CPU

→ go

← descriptor

← data

← interrupt

device
Relatively modern HW looks like this below

"North Bridge"
CPU has VMs and VAs

PCI doesn't so 1/0 generally deals with physically Addrs