I/O and DMA

memory

Frame Buffer

data lines

address lines

Fxxx → Frame buffer

Effx, RAM (0000)

~3GHz

1 cycle

L1

L2 / L3

RAM

PCI

1000

Memory

I/O registers

head

tail

DMA Descriptor

command

len

status

7 prepare DMA descriptor

7 put & descr in circular buffer

7 update head register

CPU device

go

descriptor

data

interrupt

User

read()

Kernel

write() signal()

Device

interrupt

Interrupt

Device
(Q3) bool mbusy
    Const Cl
    ml:
        if mbusy
            unit c
            mbusy = T
        ?
    mbusy = F
    Signal Cl
    count = 0
    sum = 0
    average = 0
    count = 0
    sum = 0
    return average
    count++
    sum += x
    if count < 3
        unit c
        broadcast c
        count = 0
        average = sum / 3
        sum = 0
        return average