# Panagiotis (Pete) Manolios

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## Education

**Ph.D.** in Computer Sciences, The University of Texas at Austin, 2001.
**M.A.** in Computer Sciences, Brooklyn College, 1992.
**B.S.** in Computer Sciences, Brooklyn College, 1991.

## Employment History

**Associate Professor**. 8/2007–present.
College of Computer and Information Science, Northeastern.

**Assistant Professor**. 8/2001–present.
College of Computing, Georgia Institute of Technology.

**Adjunct Assistant Professor**. 8/2003–present.
School of Electrical and Computer Engineering, Georgia Institute of Technology.

**Research and Teaching Assistant**. 9/1995–8/2001.
Department of Computer Sciences, University of Texas at Austin.

**Summer Research Staff Member**. 5/1998–7/1998.
Digital Systems Research Center, Palo Alto.

**Adjunct Faculty**. 1/1992–6/1994.
Department of Computer and Information Science. Brooklyn College.

## Research Interests

My main research interest is mechanized formal verification and validation. What guides my research is the vision that formal methods can be used to revolutionize the design and implementation of highly reliable, robust, secure, and scalable systems in a variety of important application areas, ranging from large-scale component-based software systems to hardware systems to aerospace systems to computational biology to public health. To this end, I develop algorithms, methodologies, and concepts to formally and mechanically reason about systems. I have also devoted much of my research to applications and to building and experimentally validating tools. My other areas of interest include programming languages, distributed computing, logic, software engineering, algorithms, computer architecture, aerospace, and pedagogy.

## I. TEACHING

### A. Courses Taught

| Semester/Year | Course | Number of Students | Notes |
|---|---|---|---|
| Fall 2006 | CS 8801 SPARC Seminar | 17 | |
| Spring 2006 | CS 8803 Computational Logic | 13 | |
| Spring 2005 | CS 8803 Computational Logic | 11 | Redesigned Course |
| Spring 2005 | CS 3510 Algorithms | 59 | |
| Fall 2004 | CS 8801 Hardware Verification | 7 | New; cross-listed ECE 8801 |
| Spring 2004 | CS 3500 Theory I | 60 | |
| Spring 2004 | CS 8803 Formal Methods | 18 | Cross-listed ECE 8823 B |
| Spring 2003 | CS 8803 Formal Methods | 10 | |
| Fall 2002 | CS 3220 Processor Design | 34 | Redesigned Course |

| Semester/Year | Course | Number of Students | Notes |
|---|---|---|---|
| Spring 2002 | CS 8803 Formal Modeling and Analysis of Computing Systems | 12 | New Course |
| Summer 1994 | Introduction to Mathematical Reasoning and Computer Science | 19 | |
| Spring 1994 | Introduction to Mathematical Reasoning and Computer Science | 35 | |
| Spring 1994 | Computer Organization | 27 | |
| Fall 1993 | Computer Organization | 14 | |
| Fall 1993 | Introduction to Computing Using Pascal | 38 | |
| Summer 1993 | Computer Organization | 12 | |
| Summer 1993 | Microcomputer Business Applications | 23 | |
| Spring 1993 | Computer Organization | 26 | |
| Spring 1993 | Introduction to Mathematical Reasoning and Computer Science | 37 | |
| Fall 1992 | Data Structures | 26 | |
| Fall 1992 | Introduction to Mathematical Reasoning and Computer Science | 40 | |

**B. Curriculum Development**

CS 4560: Verification of Systems. This undergraduate course was developed with Alex Orso for the Georgia Tech threads program in Fall 2005. The course provides an introduction to the basic methods and tools for verifying and validating computing systems. Students will acquire a clear understanding of the core issues in verification and validation and learn how to prioritize, conduct, and evaluate verification and validation efforts. Topics covered will include: modeling of systems, model checking, decision procedures, theorem proving, testing, runtime verification, evaluation, and certification.

CS 6382: Computational Logic. This graduate course, offered starting Spring 2005, is a refinement of the Formal Modeling and Analysis of Computing Systems course. The class is a breadth course in Software Engineering and Information Security. Much of the material is part of the Software Engineering and Programming Language qualifiers. This class provides a graduate-level introduction to the fundamental ideas in modern logic that underlie computing. Topics covered include first-order logic, Gödel's completeness and incompleteness theorems, decision problems in first-order logic, mechanical verification, modeling computing systems, formal semantics of programming languages, decision procedures, temporal logic, model checking, abstraction, and refinement.

CS 8801: Hardware Verification. New graduate seminar (Spring 2004) on current research on modeling and formally verifying hardware. Half of the semester is devoted to introducing the topic, including: an introduction to the ACL2 theorem proving system, which we use to model DLX-like machines; an introduction to correctness criteria focusing on recent work on refinement; the use of ACL2 to prove the DLX machine correct; and a discussion of decision procedures, including SAT-solvers and solvers for fragments of first-order logic with uninterpreted functions. The rest of the semester consists of student presentations on current research topics based on student interest.

CS 8803: Formal Modeling and Analysis of Computing Systems. New graduate course (Spring 2002) on the fundamental techniques for modeling and formally analyzing computing systems, with a focus on applications in software, hardware, and security. Students learn the fundamentals of classical logic, induction and recursion, program semantics, rewriting, reactive systems, temporal

logic, model checking, and abstraction. We examine how these methods can be used to verify software, hardware, and security protocols. Students learn how to use various tools, including theorem proving and model checking tools, and work in groups to apply the tools to various domains. We discuss the limitations of current techniques and systems and we examine promising research directions including building more useful systems and developing more powerful techniques.

CS 3220: Processor Design. This is a junior-level undergraduate course where students use FPGAs to design and build a microprocessor at the bit level. We distribute the FPGAs and associated software to all the students for the duration of the semester. This allows us to assign in-depth projects that provide invaluable engineering experience and insight that is difficult to impart without the constant availability of the FPGAs. The class also provides an in-depth treatment of verification.

**C. Individual Student Guidance**

1. Research Scientists Supervised

   Carlos Pacheco. October 2001-August 2002, currently a PhD student at MIT.

2. Ph.D. Students Supervised

   **Daron Vroon:** January 2002-August 2007. Daron successfully defended on August 7, 2007.
   **Research:** B.24, B.22, B.20, B.11, B.6, D.7, D.4, F.11, F.10, F.4, H.7, H.6, H.5, and H.1.
   **Notes:** Daron was the recipient of an NSF Graduate Research Fellowship.

   **Sudarshan Kumar Srinivasan:** Fall 2003-August 2007, Sudarshan successfully defended on August 10, 2007.
   **Research:** B.24, B.19, B.18, B.17, B.15, B.14, B.13, B.10 D.6, D.5, D.1.2, F.7, F.3, G.3, and H.7
   **Notes:** Sudarshan has accepted a position as an assistant professor (tenure track) at North Dakota State University.

   **Peter Dillinger:** Fall 2003-Present, Expected graduation: TBD.
   **Research:** B.12, F.10, F.8, F.5, H.5, H.3, and H.2
   **Notes:** Peter was accorded an honorable mention for his NSF Graduate Research Fellowship application.

3. Other Ph.D. Special Problems Students

   Viswanath Nagarajan (Fall 2003), Christoph Csallner (Fall 2003), Shan Shan Huang (Fall 2003), Kemin Yang (Spring & Summer 2003), David Dagon (Spring 2003), Tom Bankston (Fall 2002), and Jim Bowring (Spring 2002).

4. Masters Students Supervised

   **Roma Kane:** Spring 2005-Present, Graduated with a masters degree in Spring 2007.
   **Research:** B.19.

   **Gayatri Subramanian:** Spring 2005-Spring 2006, Graduated Spring 2006.
   **Research:** H.6.
   **Notes:** Graduated with a Master's thesis under my supervision, entitled "Automating Component-Based System Assembly."

5. Other M.S. Special Problems Students

   Christopher Church (Fall 2004), Ivan Raikov (Fall 2004)

6. Undergraduate Special Problems Students

   Numan Salati (Summer 2003), Lazy Rewriting. Phu C. Le (Fall 2004) Processor Verification. Daniel E. Vogh (Fall 2005) ACL2 and compiler verification. Denis Bueno (Spring 2006-Spring 2007) Expressive Package Management.

7. Visiting Special Problems Students

   Marc Galceran Oms [see B.25] (Spring-Summer 2006) and Sergi Oliva Valls [see B.25] (Spring 2006) Using SAT solving techniques for computational biology.

## II. RESEARCH AND CREATIVE SCHOLARSHIP

### A. Dissertation

1. Panagiotis Manolios. Mechanical Verification of Reactive Systems. The University of Texas at Austin, Department of Computer Sciences, Austin, TX, August 2001.

### B. Conference Papers

29. Panagiotis Manolios, Sudarshan Srinivasan, and Daron Vroon. BAT: The Bit-Level Analysis Tool. *CAV 2007, Nineteenth International on Computer Aided Verification*, to appear. Springer, July 2007.

28. Panagiotis Manolios, Gayatri Subramanian, and Daron Vroon. Automating Component-Based System Assembly. *ISSTA 2007, International Symposium on Software Testing and Analysis*, to appear. ACM, July 2007.

27. Panagiotis Manolios and Daron Vroon. Efficient Circuit to CNF Conversion. *SAT 2007, The Tenth International Conference on Theory and Applications of Satisfiability Testing*, to appear. Springer, May 2007.

26. Peter Dillinger, Panagiotis Manolios, J S. Moore, Daron Vroon. ACL2s: "The ACL2 Sedan." *ICSE'07, The 29th International Conference on Software Engineering, Research Demonstration Track*, to appear. ACM, May 2007.

25. Panagiotis Manolios, Marc Galceran Oms, and Sergi Oliva Valls. Checking Pedigree Consistency with SAT. *TACAS 2007, International Conference on Tools and Algorithms for the Construction and Analysis of Systems*. Springer, March 2007. (26% acceptance rate, 54 out of 204; this is a tools paper, so the acceptance rate is probably higher)

24. Panagiotis Manolios, Sudarshan K. Srinivasan, and Daron Vroon. Automatic Memory Reductions for RTL-Level Verification. *ICCAD 2006, ACM-IEEE International Conference on Computer Aided Design*. IEEE Computer Society, November 2006. (24% acceptance rate, 130 out of 537; the acceptance rate for long papers, like ours, is lower)

23. William G.J. Halfond, Alessandro Orso, and Panagiotis Manolios. Using Positive Tainting and Syntax-Aware Evaluation to Counter SQL Injection Attacks. *The Twelfth ACM SIGSOFT Symposium on Foundations of Software (FSE'06)*. ACM, November 2006. (20% acceptance rate, 25 out of 125)

22. Panagiotis Manolios and Daron Vroon. Termination Analysis with Calling Context Graphs. *Computer-Aided Verification (CAV-2006)*, volume 4144 of *LNCS*, pages 401–414. Springer, August 2006. (28% acceptance rate for regular papers, 35 out of 121)

21. Panagiotis Manolios and Yimin Zhang. Implementing Survey Propagation on Graphics Processing Units. *Ninth International Conference on Theory and Applications of Satisfiability Testing (SAT-2006)*, volume 4121 of *LNCS*, pages 311–324. Springer, August 2006. (34% acceptance rate for regular papers, 26 out of 75)

20. Panagiotis Manolios and Daron Vroon. Integrating Static Analysis and General-Purpose Theorem Proving for Termination Analysis. *ICSE'06, The 28th International Conference on Software Engineering, Emerging Results*, pages 873–876. ACM, May 2006. (33% acceptance rate, 22 out of 65)

19. Roma Kane, Panagiotis Manolios, and Sudarshan K. Srinivasan. Monolithic Verification of Deep Pipelines with Collapsed Flushing. *DATE 2006, ACM-IEEE Design, Automation, and Test in Europe*, pages 1234-1239. European Design and Automation Association, March 2006. (27% acceptance rate, 233 out of 834; the acceptance rate for long papers, like ours, is lower)

18. Panagiotis Manolios and Sudarshan K. Srinivasan. Verification of Executable Pipelined Machines with Bit-Level Interfaces. *ICCAD 2005, ACM-IEEE International Conference on Computer Aided Design*, pages 855–862. IEEE Computer Society, November 2005. (23% acceptance rate, 128 out of 540; the acceptance rate for long papers, like ours, is lower)

17. Panagiotis Manolios and Sudarshan K. Srinivasan. A Complete Compositional Reasoning Framework for the Efficient Verification of Pipelined Machines. *ICCAD 2005, ACM-IEEE International Conference on Computer Aided Design*, pages 863–870. IEEE Computer Society, November 2005. (23% acceptance rate, 128 out of 540; the acceptance rate for long papers, like ours, is lower)

16. Panagiotis Manolios. The Challenge of Hardware-Software Co-Verification. *VSTTE, IFIP Working Conference on Verified Software: Theories, Tools, Experiments, Part of ETH's 150th anniversary celebration.* Zurich, October 2005.

15. Panagiotis Manolios and Sudarshan K. Srinivasan. A Parameterized Benchmark Suite of Hard Pipelined-Machine-Verification Problems. *Advanced Research Working Conference on Correct Hardware Design and Verification Methods (CHARME 2005)*, volume 3725 of *LNCS*, pages 363–366. Springer, October 2005.

14. Panagiotis Manolios and Sudarshan K. Srinivasan. A Computationally Efficient Method Based on Commitment Refinement Maps for Verifying Pipelined Machines. *ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE 2005)*, pages 188-197. IEEE, July 2005. (36% acceptance rate; 17 out of 47 papers)

13. Panagiotis Manolios and Sudarshan K. Srinivasan. Refinement Maps for Efficient Verification of Processor Models. *DATE 2005, Design, Automation, and Test in Europe*, pages 1304–1309. IEEE Computer Society, March 2005. (21% acceptance rate, 176 out of 825; the acceptance rate for long papers, like ours, is lower)

12. Peter C. Dillinger and Panagiotis Manolios. Bloom Filters in Probabilistic Verification. *Formal Methods in Computer-Aided Design (FMCAD 2004)*, volume 3312 of *LNCS*, pages 367–381. Springer, November 2004. (42% acceptance rate, 29 out of 69)

11. Panagiotis Manolios and Daron Vroon. Integrating Reasoning about Ordinal Arithmetic into ACL2. *Formal Methods in Computer-Aided Design (FMCAD 2004)*, volume 3312 of *LNCS*, pages 82–97. Springer, November 2004. (42% acceptance rate, 29 out of 69)

10. Panagiotis Manolios and Sudarshan K. Srinivasan. Automatic Verification of Safety and Liveness for XScale-Like Processor Models Using WEB Refinements. *Design, Automation, and Test in Europe (DATE 2004)*, pages 168–175. IEEE Computer Society, February 2004. (17% acceptance rate for long papers)

9. Panagiotis Manolios. A Compositional Theory of Refinement for Branching Time. *CHARME 2003, the 12th Advanced Research Working Conference on Correct Hardware Design and Verification Methods*, volume 2860 of *LNCS*, pages 304–318. Springer, October 2003. (36% acceptance rate, 24 out of 65)

8. Panagiotis Manolios and Richard Trefler. A Lattice-Theoretic Approach to Safety and Liveness. *Twenty-Second ACM Symposium on Principles of Distributed Computing (PODC 2003)*, pages 325–333. ACM Press, July 2003. (16% acceptance rate, 35 out of 208)

7. Panagiotis Manolios. Branching Time Refinement. Brief Announcements, *Twenty-Second ACM Symposium on Principles of Distributed Computing (PODC 2003)*, pages 334–334. ACM Press, July 2003.

6. Panagiotis Manolios and Daron Vroon. Algorithms for Ordinal Arithmetic. *Nineteenth International Conference on Automated Deduction (CADE)*, volume 2741 of *LNCS*, pages 243–257. Springer, July 2003. (34% acceptance rate, 29 out of 83)

5. Panagiotis Manolios and Richard Trefler. Safety and liveness in branching time. In Joseph Halpern, editor, *Logic in Computer Science–LICS 2001*, pages 366–374. IEEE Computer Society, June 2001. (36% acceptance rate, 36 out of 104)

4. Panagiotis Manolios. Correctness of pipelined machines. In Warren A. Hunt, Jr. and Stephen D. Johnson, editors, *Formal Methods in Computer-Aided Design–FMCAD 2000*, volume 1954 of *LNCS*, pages 161–178. Springer, November 2000. (47% acceptance rate, 30 out of 63)

3. Panagiotis Manolios, Kedar Namjoshi, and Robert Sumners. Linking theorem proving and model-checking with well-founded bisimulation. In Nicolas Halbwachs and Doron Peled, editors, *Computer-Aided Verification–CAV '99*, volume 1633 of *LNCS*, pages 369–379. Springer, July 1999. (31% acceptance rate, 34 out of 107)

2. Yuan Yu, Panagiotis Manolios, and Leslie Lamport. Model checking $\mathrm{TLA}^+$ specifications. In Laurence Pierre and Thomas Kropf, editors, *Correct Hardware Design and Verification Methods, CHARME '99*, volume 1703 of *LNCS*, pages 54–66. Springer, September 1999. (41% acceptance rate, 20 out of 48)

1. Don L. Scarborough, Panagiotis Manolios, and Jacqueline A. Jones. MusicSoar: Soar as an architecture for music cognition. In *Proceedings of the Fourteenth Annual Conference of the Cognitive Science Society*, pages 1104–1109, July 1992.

**C. Books**

6. Aarti Gupta and Panagiotis Manolios, editors. *Proceedings of the ACM/IEEE Formal Methods in Computer-Aided Design Conference.* IEEE, November 2006. (22% acceptance rate; 91 regular papers submitted, 20 accepted)

5. Panagiotis Manolios and Matthew Wilding, editors. *Proceedings of the Sixth International Workshop on the ACL2 Theorem Prover and its Applications.* ACM, August 2006.

4. Matt Kaufmann, Panagiotis Manolios, and J Strother Moore. *Computer-Aided Reasoning: An Approach.* Paperback Edition (of C.2), August 2002.

   Note: this is the ACL2 textbook. ACL2 is part of the Boyer-Moore family of provers, winner of the 2005 ACM Software System Award.

3. Matt Kaufmann, Panagiotis Manolios, and J Strother Moore, editors. *Computer-Aided Reasoning: ACL2 Case Studies.* Paperback Edition (of C.1), August 2002.

2. Matt Kaufmann, Panagiotis Manolios, and J Strother Moore. *Computer-Aided Reasoning: An Approach.* Kluwer Academic Publishers, July 2000.

1. Matt Kaufmann, Panagiotis Manolios, and J Strother Moore, editors. *Computer-Aided Reasoning: ACL2 Case Studies.* Kluwer Academic Publishers, June 2000.

**D. Journal Articles**

9. Panagiotis Manolios and Richard Trefler. A Semantic Characterization of Safety and Liveness for Branching Time Logics, 41 pages. *To appear. Distributed Computing*.

8. William G.J. Halfond, Alessandro Orso, and Panagiotis Manolios. WASP: Detecting and Preventing SQL Injection Attacks Using Positive Tainting and Syntax-Aware Evaluation, 37 pages. *To appear. IEEE Transactions on Software Engineering, special issue on Software Engineering for Secure Systems*.

7. David A. Greve, Matt Kaufmann, Panagiotis Manolios, J S. Moore, Sandip Ray, Jose L. Ruiz-Reina, Rob Sumners, Daron Vroon, and Matthew Wilding. Efficient Execution in an Automated Reasoning Environment, 32 pages. *To appear. Journal of Functional Programming*. (See also Technical Report G.4)

6. Panagiotis Manolios and Sudarshan K. Srinivasan. Automatic Verification of Safety and Liveness for Pipelined Machines Using WEB Refinement, 18 pages. *Accepted pending minor revisions, which we have made and submitted. ACM Transactions on Design Automation of Electronic Systems*.

5. Panagiotis Manolios and Sudarshan K. Srinivasan. A Framework for Verifying Bit-Level Pipelined Machines Based on Automated Deduction and Decision Procedures, 26 pages. *Journal of Automated Reasoning*, volume 37(1–2), pages 93–116, 2006.

4. Panagiotis Manolios and Daron Vroon. Ordinal Arithmetic: Algorithms and Mechanization. *Journal of Automated Reasoning*, volume 34(4), pages 387–423, 2005.

3. Panagiotis Manolios and J Strother Moore. Partial Functions in ACL2. *Journal of Automated Reasoning*, volume 31(2), pages 107–127, 2003.

2. Panagiotis Manolios and J Strother Moore. On the desirability of mechanizing calculational proofs. *Information Processing Letters*, 77(2–4): 173–179, January 2001.

1. Panagiotis Manolios and Robert Fanelli. First order recurrent neural networks and deterministic finite automata. *Neural Computation*, volume 6, pages 1155–1173, MIT Press, November 1994.

**D.1 Submitted Journal Articles**

1. Panagiotis Manolios and Sudarshan K. Srinivasan. A Refinement-Based Compositional Reasoning Framework for Pipelined Machine Verification, 13 pages. *Submitted to IEEE Transactions on VLSI Systems*.

**E. Book Chapters**

2. Panagiotis Manolios. Refinement and Theorem Proving. *Formal Methods for Hardware Verification*, volume 3965 of *LNCS*, pages 176–210. Springer, May 2006.

1. Panagiotis Manolios. Mu-calculus model-checking. In Matt Kaufmann, Panagiotis Manolios, and J Strother Moore, editors, *Computer-Aided Reasoning: ACL2 Case Studies*, pages 93–111. Kluwer Academic Publishers, June 2000.

**F. Refereed Workshop Papers**

12. Peter Dillinger, Matt Kaufmann, and Panagiotis Manolios. Hacking and Extending ACL2. *Seventh International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2 2007)*, November 2007.

11. Matt Kaufmann, Panagiotis Manolios, J S. Moore, and Daron Vroon. Integrating CCG Analysis into ACL2. *The Eight International Workshop on Termination*, part of FLoC'06, August 2006.

10. Peter C. Dillinger, Panagiotis Manolios, J S. Moore, and Daron Vroon. ACL2s: "The ACL2 Sedan". *User Interfaces for Theorem Provers Workshop*, part of FLoC'06, August 2006.

9. Panagiotis Manolios. Automating the Verification of RTL-Level Pipelined Machines. *DCC'06, The Seventh International Workshop on Designing Correct Circuits*, April, 2006.

8. Peter C. Dillinger and Panagiotis Manolios. Enhanced Probabilistic Verification with 3Spin and 3Murphi. *SPIN 2005, 12th International SPIN Workshop on Model Checking of Software*, volume 3639 of *LNCS*, pages 272–276. Springer, August 2005.

7. Panagiotis Manolios and Sudarshan Srinivasan. A Suite of Hard ACL2 Theorems Arising in Refinement-Based Processor Verification. *Fifth International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2 2004)*. November 2004.

6. Marcio Gameiro and Panagiotis Manolios. Formally Verifying an Algorithm Based on Interval Arithmetic for Checking Transversality. *Fifth International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2 2004)*, November 2004.

5. Peter C. Dillinger and Panagiotis Manolios. Fast *and* Accurate Bitstate Verification for SPIN. *SPIN 2004, 11th International SPIN Workshop on Model Checking of Software*, volume 2989 *LNCS*, pages 57–75. Springer-Verlag, April 2004.

4. Panagiotis Manolios and Daron Vroon. Ordinal Arithmetic in ACL2. *Fourth International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2-2003)*, July 2003.

3. Panagiotis Manolios and Matt Kaufmann. Adding a Total Order to ACL2. In Matt Kaufmann and J Strother Moore, editors, *The Third International Workshop on the ACL2 Theorem Prover*. April 2002.

2. Panagiotis Manolios and J Strother Moore. Partial functions in ACL2. In Matt Kaufmann and J Strother Moore, editors, *Proceedings of the ACL2 Workshop 2000*. October 2000.

1. Panagiotis Manolios. Verification of pipelined machines in ACL2. In Matt Kaufmann and J Strother Moore, editors, *Proceedings of the ACL2 Workshop 2000*. October 2000.

**G. Technical Reports**

4. David A. Greve, Matt Kaufmann, Panagiotis Manolios, J S. Moore, Sandip Ray, Jose L. Ruiz-Reina, Rob Sumners, Daron Vroon, and Matthew Wilding. Efficient Execution in an Automated Reasoning Environment. The University of Texas at Austin, Department of Computer Sciences. Technical Report TR-06-59. November 20, 2006. 53 pages. (Expanded version of Journal paper D.7)

3. Panagiotis Manolios and Sudarshan K. Srinivasan. Automatic Verification of Safety and Liveness for XScale-Like Processor Models Using WEB-Refinements. CERCS TR# GIT-CERCS-03-17, September 2003. (Corresponds to Conference paper B.10)

2. Panagiotis Manolios. Enumerating the strings of a regular expression. Technical Report TR2000-30, Department of Computer Sciences, The University of Texas at Austin, December 2000.

1. Panagiotis Manolios, Kedar Namjoshi, and Robert Sumners. Linking theorem proving and model-checking with well-founded bisimulation. Technical Report TR-99-02, Department of Computer Sciences, The University of Texas at Austin, January 1999.

**H. Software**

7. Panagiotis Manolios, Sudarshan Srinivasan, and Daron Vroon. BAT, The Bit-level Analysis Tool, is a bounded model checker that can be used to verify properties of models written in the BAT language, a strongly typed language with three different kinds of types: bit vectors, memories, and multiple value types. BAT also allows user-defined functions and performs type inference. Overall, it makes it very convenient to define hardware models at the bit level. One of the novel aspects of BAT is that it implements a new sound and complete memory abstraction algorithm that allows us to reduce the size of addresses and a technique for simplifying memories that combines term-rewriting with SAT solving. BAT can automatically verify bit-level pipelined machine designs beyond the reach of other state-of-the-art methods.

6. Panagiotis Manolios, Gayatri Subramanian, and Daron Vroon. CoBaSA, Component Based System Assembly, is a tool for automatically solving one of the major challenges in the development of large component-based software systems, namely the system assembly problem: which components should be selected and how should they be connected, integrated, and assembled so that the overall system requirements are satisfied? CoBaSA includes an expressive language for declaratively describing system-level requirements, component interfaces and dependencies, resource requirements, safety properties, objective functions, and various types of constraints, including replication, timing, scheduling, and separation constraints (among others). We then automatically solve the system assembly problem using constraint solving techniques that take advantage of current SAT-based methods. CoBaSA is being successfully applied to several large-scale industrial examples involving the Boeing 787 Dreamliner.

5. Peter Dillinger, Panagiotis Manolios, and Daron Vroon. ACL2s. This is a version of the ACL2 theorem proving system (winner of the 2005 ACM Software System Award) designed to make formal reasoning more widely accessible. To this end, we have developed a modern integrated development environment using Eclipse; we developed and implemented several abstractions that enable users to quickly determine the state of the theorem prover; and we have developed and implemented algorithms and techniques for simplifying the logic and user interactions with the theorem prover (*e.g.*, by providing powerful termination analysis methods). ACL2s has been downloaded over 750 times.

4. Panagiotis Manolios. Bloom Filter Calculator. I developed a Web application to enable users of Bloom filters to optimally configure the data structure for their applications. The tool has

been used over 15,000 times by a wide variety of users. The tool is available online at `http://www.cc.gatech.edu/ manolios/bloom-filters/calculator.html`.

3. Peter Dillinger and Panagiotis Manolios. We developed a new version of SPIN, called 3SPIN. SPIN is a popular model checking tool that can be used for the formal verification of distributed software systems. The tool was developed at Bell Labs by Gerard Holzmann in the original Unix group of the Computing Sciences Research Center, starting in 1980, and continues to evolve to keep pace with new developments in the field. In April 2002 the tool was awarded the prestigious System Software Award for 2001 by the ACM. Our 3SPIN provides significant improvements with regard to the utilization of Bloom filters. Peter Dillinger worked with Holzmann at NASA JPL as a summer intern and some of these improvements have subsequently been added to SPIN.

2. Peter Dillinger and Panagiotis Manolios. We developed a new version of Murphi, called 3Murphi. Murphi is a popular model checking tool developed at Stanford University by David Dill's group. Our modifications enhance the probabilistic algorithms and data structures for storing visited states, making them more effective and more usable for verifying huge transition systems. 3Murphi also supports a verification methodology designed to minimize time to finding errors, or to reaching a desired certainty that no errors exist. 3Murphi and 3SPIN are the only tools to offer this support, and do so with the most powerful and flexible currently-available implementations of the underlying algorithms and data structures.

1. Panagiotis Manolios and Daron Vroon. We modified ACL2's logic, specifically the internal representation and handling of the ordinals. We also added a powerful library of definitions and theorems about ordinal arithmetic and modified the extensive corpus of ACL2 case studies to conform. Our modifications have appeared in every version of ACL2 since version 2.8 (released in March 2004). ACL2 is a widely used system that was recently awarded the prestigious 2005 ACM Software System Award.

**I. Research Proposals and Grants**

12. **Hierarchical Component-Based Framework for the Formal Verification and Validation of Complex Aerospace Software Systems**
NASA, Aviation Safety: Integrated Vehicle Health Management Project
PI: Panagiotis Manolios
Co-PIs: Eric Feron (Georgia Tech, Aerospace), Cesar Munoz (National Institute of Aerospace), Arnaud Venet (Kestrell Technology)
Amount: $1,568,750, February 2007

11. **Software Verification: Common Computing System Hosted Function Allocation Automation and Modeling/Analysis of Fault Propagation**
Boeing Aerospace Company
Co-PI with Mary Jean Harrold
Amount: $250,000, January 2007
Note: This is to continue the 2006 work.

10. **Software Verification: Common Computing System Hosted Function Allocation Automation and Modeling/Analysis of Fault Propagation**
Boeing Aerospace Company
Co-PI with Mary Jean Harrold
Amount: $250,000, January 2006

9. **Software Verification: Hosted Function Allocation Automation and Fault Propagation Analysis**

Boeing Aerospace Company
Co-PI with Mary Jean Harrold
Amount: $180,000, February 2005

8. **An Eclipse-Based Integrated Development Environment for Integrating Computer-Aided Reasoning into the Computer Science Curriculum**
   IBM, Eclipse Innovation Grant
   Amount: $15,000, 2005

7. **SoD: Collaborative: Language towers as design frameworks**
   NSF, Science of Design Program
   PI: Olin Shivers
   CO-PIs: Panagiotis Manolios and Matthew Flatt (University of Utah)
   Amount: $450,000 for Georgia Tech, $629,999 in total, January 2005

6. **Software Verification Through Interface Analysis and Change Impact Analysis**
   Boeing Aerospace Company
   PI: Panagiotis Manolios
   Amount: $67,230, December 2004

5. **System-Level Processor Verification Using Refinement**
   NSF, Computing Processes & Artifacts Program
   PI: Panagiotis Manolios
   Amount: $250,000, September 2004

4. **Integrating Functional Computer-Aided Reasoning into the Computer Science Curriculum**
   NSF, CISE Combined Research and Curriculum Development and Educational Innovation Program
   PI: Panagiotis Manolios
   Co-PI's: J Moore and Olin Shivers
   Amount: $470,000, August 2004

3. **Software Verification Through Interface Analysis and Change Impact Analysis**
   Boeing Aerospace Company
   Co-PI with Mary Jean Harrold
   Amount: $180,000, January 2004

2. **Software Verification Through Interface Analysis and Change Impact Analysis**
   Boeing Aerospace Company
   Co-PI with Mary Jean Harrold
   Amount: $50,000, Fall 2003

1. **Reconfigurable Logic Kits for Hardware-Centric Courses**
   Georgia Tech, Technology Fee Funds
   Co-PI with Kenneth Mackenzie
   Amount: $25,750, August 2002

## III. SERVICE

### A. Conference Committee Activities

21. Program Committee Member, The Eleventh International Conference on Theory and Applications of Satisfiability Testing (SAT) 2008.

20. Program Committee Member, Automated Formal Methods (AFM) 2007.
19. Steering Committee Member, ACM-IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD). 2007-Present.
18. Program Committee Member, ACM-IEEE International Conference on Computer-Aided Design (ICCAD) 2007.
17. Program Committe Member and Benchmark Chair, ACM-IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD) 2007.
16. Program Committee Member, The International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2) 2007.
15. Program Committee Member, The Tenth International Conference on Theory and Applications of Satisfiability Testing (SAT) 2007.
14. Program Committee Member, Asia and South Pacific Automation Conference (ASP-DAC) 2007.
13. Program and general chair (with Aarti Gupta), ACM-IEEE Conference on Formal Methods in Computer-Aided Design (FMCAD) 2006. (91 regular papers submitted, 20 accepted, 22% acceptance rate)
12. Program and general chair (with Matt Wilding), ACM International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2) 2006.
11. Program Committee Member, ACM-IEEE International Conference on Computer-Aided Design (ICCAD) 2006.
10. Program Committee Member, Automated Formal Methods (AFM) 2006.
9. Program Committee Member, ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) 2006.
8. Program Committee Member, Advanced Research Working Conference on Correct Hardware Design and Verification Methods (CHARME) 2005.
7. Program Committee Member, International Conference on Theorem Proving in Higher Order Logics (TPHOLs) 2005.
6. Program Committee Member, The Fifth International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2) 2004.
5. Program Committee Member, Computer-Aided Verification (CAV) 2004.
4. Program Committee Member, Computer-Aided Verification (CAV) 2003.
3. Program Committee Member, International Conference on Computer Design (ICCD) 2002.
2. Program Committee Member, International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2) 2002.
1. Program Committee Member, International Workshop on the ACL2 Theorem Prover and Its Applications (ACL2) 2000.

**B. Other Reviewing**

14. Journal of the ACM (JACM)

13. Transactions on Programming Languages and Systems (TOPLAS)
12. Journal of Automated Reasoning (JAR)
11. Information Processing Letters (IPL)
10. Formal Methods in Systems Design (FMSD)
9. Design and Test (D&T)
8. Computer-Aided Verification (CAV) 1999, 2000, 2004, 2006
7. Formal Methods Europe (FME) 2001
6. Correct Hardware Design and Verification Methods (CHARME) 1999
5. International Conference on Computer Design (ICCD) 2002
4. International Conference on Software Engineering (ICSE) 2002
3. ACM Transactions on Embedded Computing Systems
2. Logic in Computer Science (LICS) 2004
1. ACM Programming Language and Implementation Conference (PLDI) 2007

**C. Project Reviewer**

2. The National Security Agency's Mathematical Sciences Program
1. NSF Panel Reviewer for the Software Engineering and Programming Languages Program, Washington DC. March 2002.

**D. Honors and Activities**

8. IBM Faculty Award for Innovation, 2005.
7. Member of the ACM, the IEEE, and the Honor Society of Phi Kapppa Phi.
6. Member of Edsger W. Dijkstra's ATAC (Austin Tuesday Afternoon Club), 1998–2001.
5. Certificate of Achievement for Outstanding Achievement in Teaching for the Year of 1998-1999 (Outstanding Teaching Assistant Award), The University of Texas at Austin, 1999.
4. NSF grant to attend the Marktoberdorf Summer School on Calculational System Design, an Advanced Study Institute of the NATO Science Committee, 1998.
3. Micro-Electronics and Computer Development Fellowship, The University of Texas at Austin, 1994-1996.
2. Awarded Certificate - Seminar on Teaching in Urban Colleges, funded by FIPSE, 1992.
1. Elected an Associate Member of Sigma Xi, The Scientific Research Society in 1992.

**E. On-campus Committees**

3. College of Computing, Computing and Systems Division, Georgia Tech. Graduate Committee. 2005-2006 Academic Year.
2. College of Computing, Core Computing Division. Steering Committee. 2003-2005 Academic Years.

1. College of Computing, Recruiting Committee. 2002-2003 Academic Year.

**F. External Committees**

3. Ph.D. Examining Committee for Jaehwan Lee, School of Electrical and Computer Engineering, Georgia Tech. Title: Hardware/Software Deadlock Avoidance for Multiprocessor Multiresource System-on-a-Chip, Oct. 2004. Advisor: Vincent J. Mooney III.

2. Masters Examining Committee for Tiffany Danielle Goble, School of Mathematics, Georgia Tech. Title: Automated Reasoning: Computer Assisted Proofs in Set Theory Using Godel's Algorithm for Class Formation, Aug. 2004. Advisor: Johan G.F. Belinfante.

1. Verified Software: Theories, Tools, Experiments. Member of panel on Tool Interoperability. Charged to come up with a report on languages and language families that can be employed for diverse tools to cooperate in solving verification problems. This is a critical issue for the Verified Software Grand Challenge. 2006.

**G. Workshops and External Courses**

4. Refinement and Theorem Proving. Lectures at SFM-06:HV, The 6th International School on Formal Methods for the Design of Computer, Communication and Software Systems: Hardware Verification. Bertinoro, Italy. May 22-27, 2006. The lectures were published by Springer Verlag, see [E.2].

3. ACL2 Tutorial for the Conference on Automated Deduction (CADE 18), part of The 2002 Federated Logic Conference (FLoC'02). Copenhagen, Denmark. July 2002.

2. ACL2 Tutorial for the European Joint Conferences on Theory and Practice of Software (ETAPS). Grenoble, France. April 2002.

1. Organizing Committee Member, ACL2 Workshop 1999.

**H. Invited Talks**

I have given about 30 invited presentations ranging from lecturing at the International School on Formal Methods to an invited talk at the NSA's High Confidence Software Systems Conference to giving colloquia at various institutions including the following: AT&T Research Labs, Brown University, Carnegie Mellon (School of Computer Science and Software Engineering Institute), Cornell, Kestrel Institute, Microsoft Research (Cambridge, Redmond, and Silicon Valley), MIT, NASA Jet Propulsion Laboratory, New York University, Northeastern University, Ohio State University, Oxford University, SRI International, University of Illinois at Urbana-Champaign, University of Michigan, University of Texas at Austin, University of Iowa, University of Utah, University of Virginia, and Washington University in St. Louis.