

Embedded Development: tmote-sky platform

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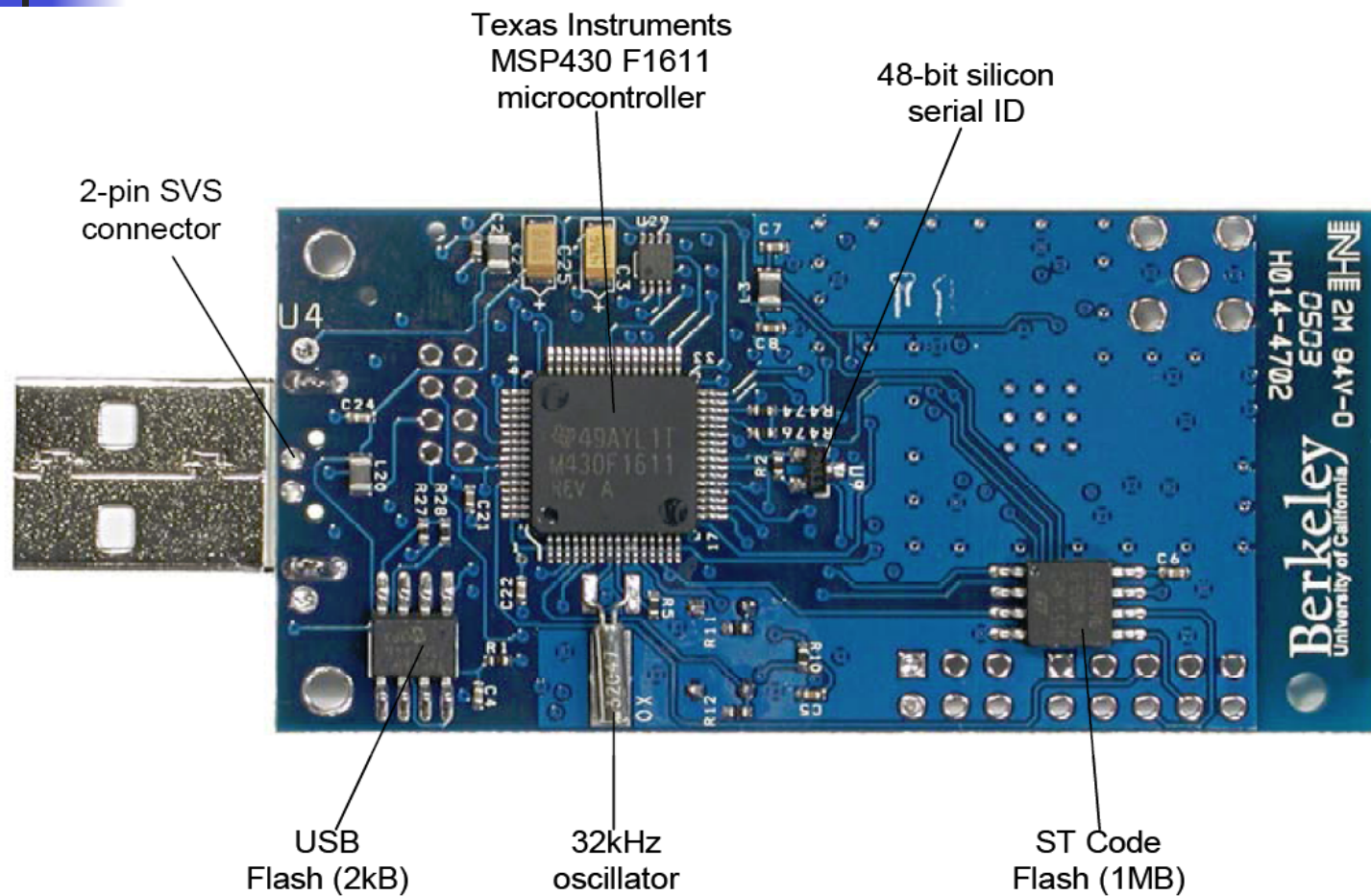
Northeastern University

Tmote Sky

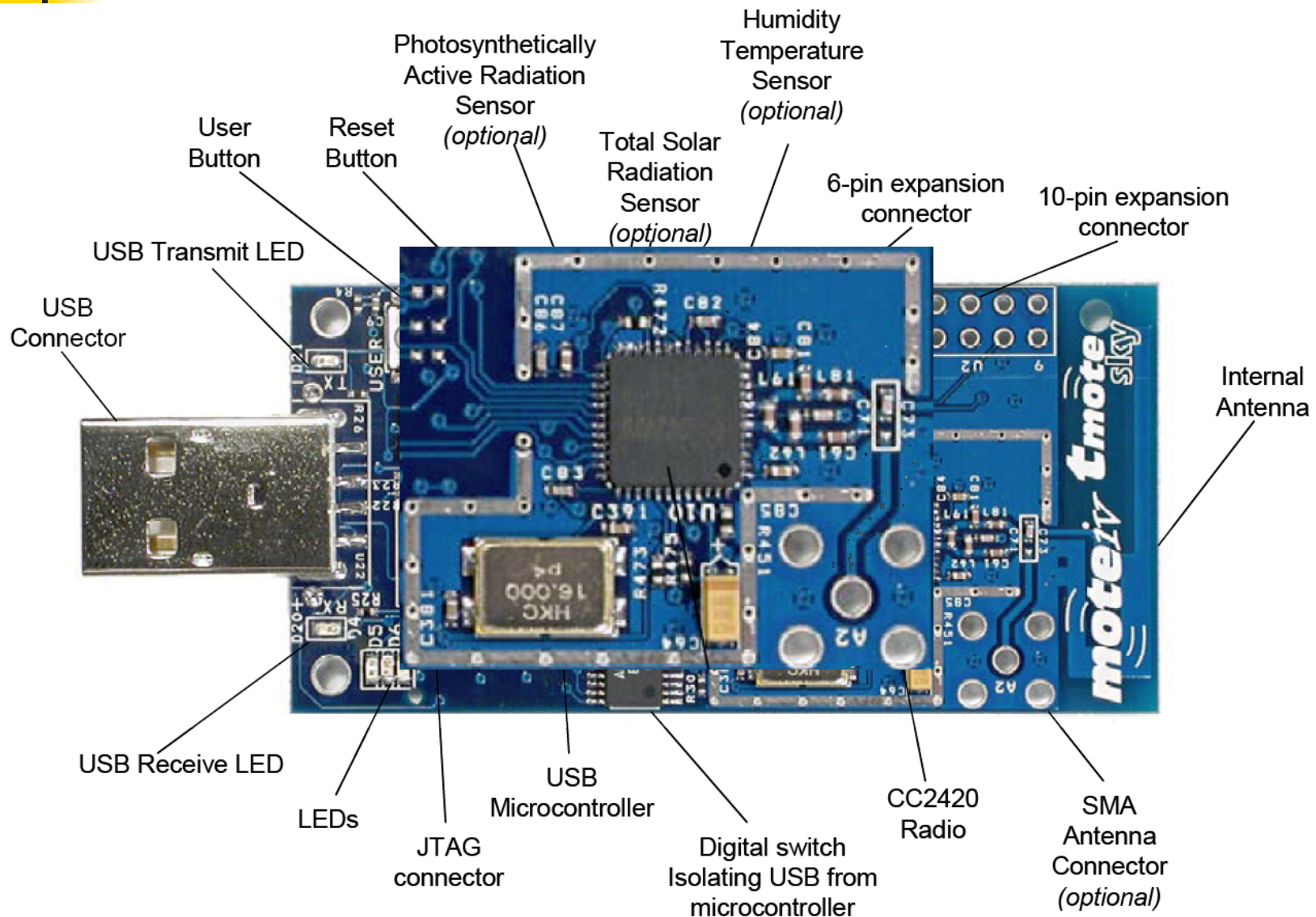


- 8MHz Texas Instruments MSP430 microcontroller (10k RAM, 48k Flash)
- 250kbps 2.4GHz IEEE 802.15.4 Chipcon Wireless Transceiver
- Integrated onboard antenna with 50m range indoors / 125m range outdoors
- Integrated Humidity, Temperature, and Light sensors
- Hardware link-layer encryption and authentication

Tmote Sky Structure (Back)



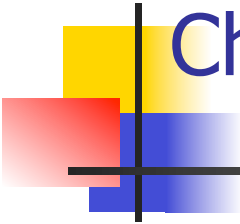
Tmote Sky Structure (Front)



Chipcon CC2420

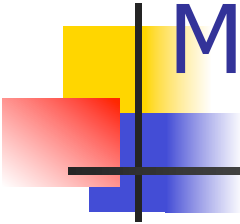


- True single-chip 2.4 GHz IEEE 802.15.4/ ZigBee RF transceiver with MAC support
- DSSS modem with 2 Mcps/s and 250 kbps effective data rate
- Programmable output power in 8 steps from -25 to 0 dBm
- Low current consumption: RX=19.7 mA; TX=17.4 mA@0dBm
- Low supply voltage (2.1 V - 3.6 V)
- Few external components
- Hardware MAC encryption and authentication (AES-128)



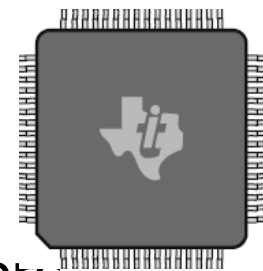
Chipcon CC2420

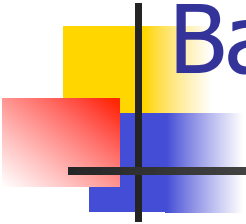
	CC2420
Frequency	2.4GHz
Data rate	250kb/s
Tx Power	-25 to 0dBm, 8 steps
Power Consumption	Tx 17.4mA@0dBm Rx 19.7mA
Rx Sensitivity	-95dBm
MAC Support	802.15.4
Encryption	AES-128



MSP430F1611

- 16-Bit RISC Architecture, up to 8 MHz
- 48KB+256B Flash Memory
- 10KB RAM
- Low Supply-Voltage Range, 1.8 V-3.6 V
- Ultralow-Power Consumption
- 2 x 16-bit Timers
- 2 x Serial Communication Interfaces
- 8 x 12-Bit A/D Converter & 2 x D/A Converters

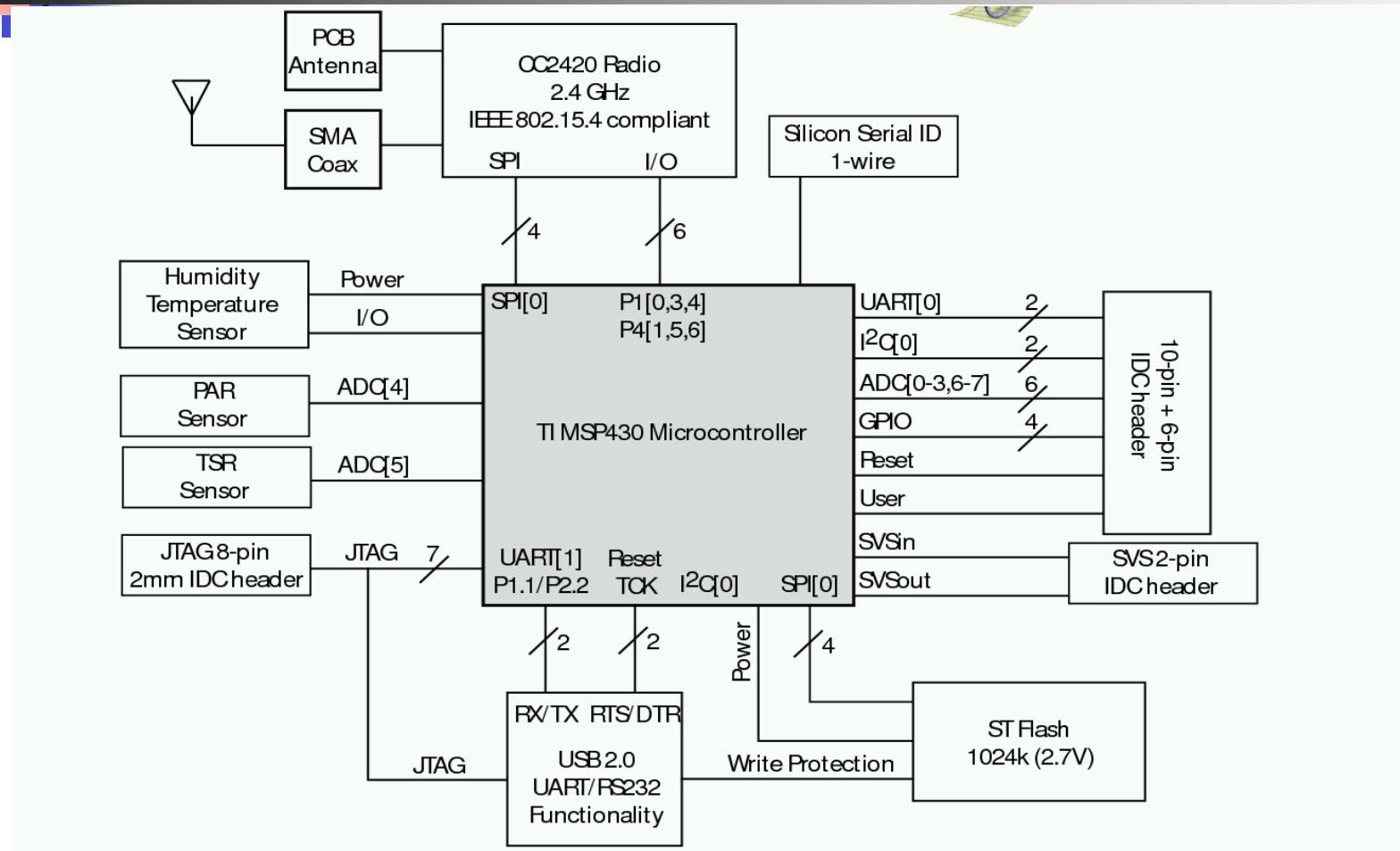


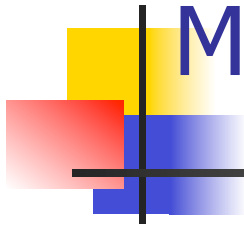


Basic Commands

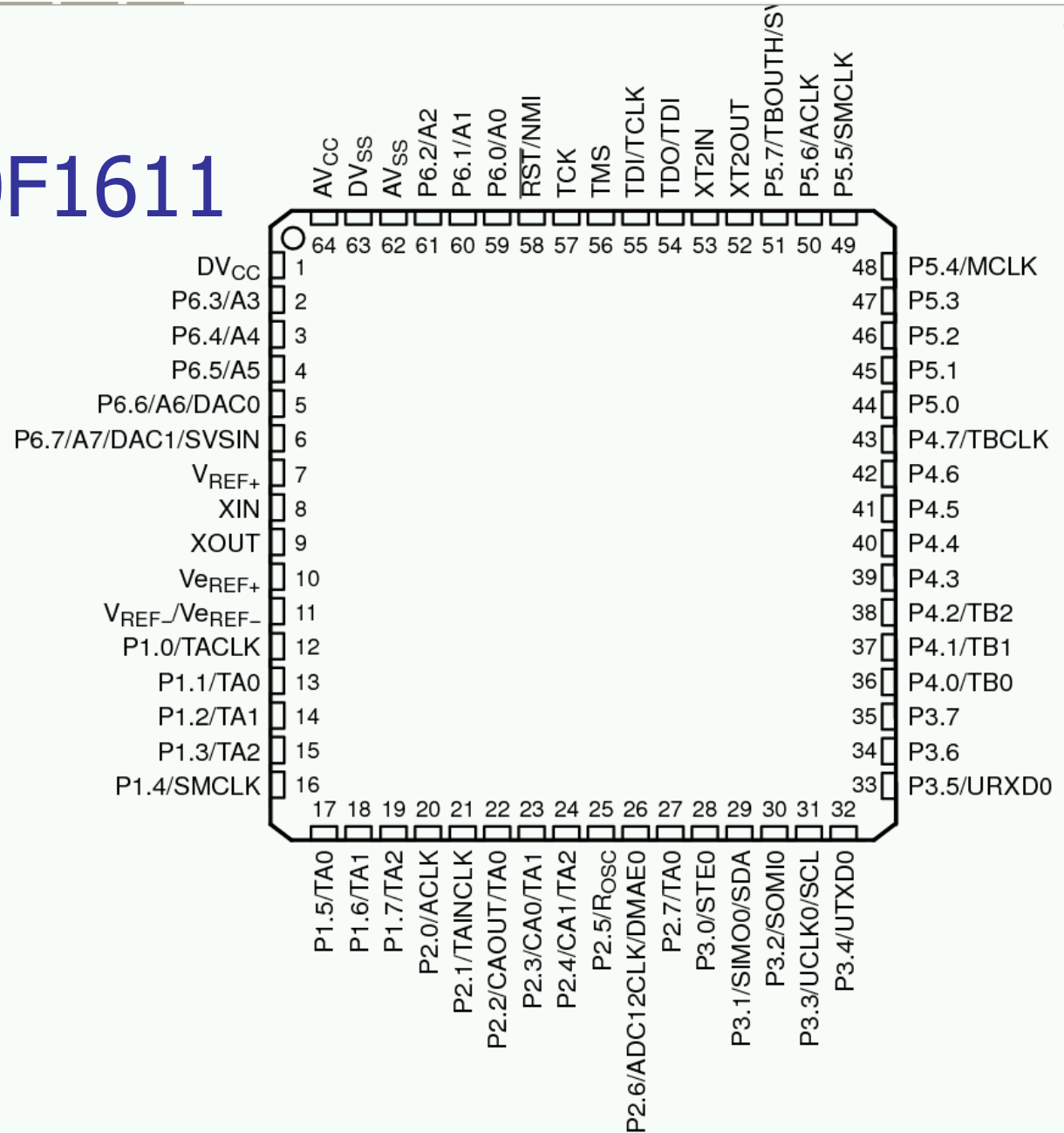
- `motelist`
- `msp430-gcc`
- `msp430-bsl.exe --telosb -c 16 -r -e
-I -p ${NAME}.a43`

Tmote-sky Block Diagram

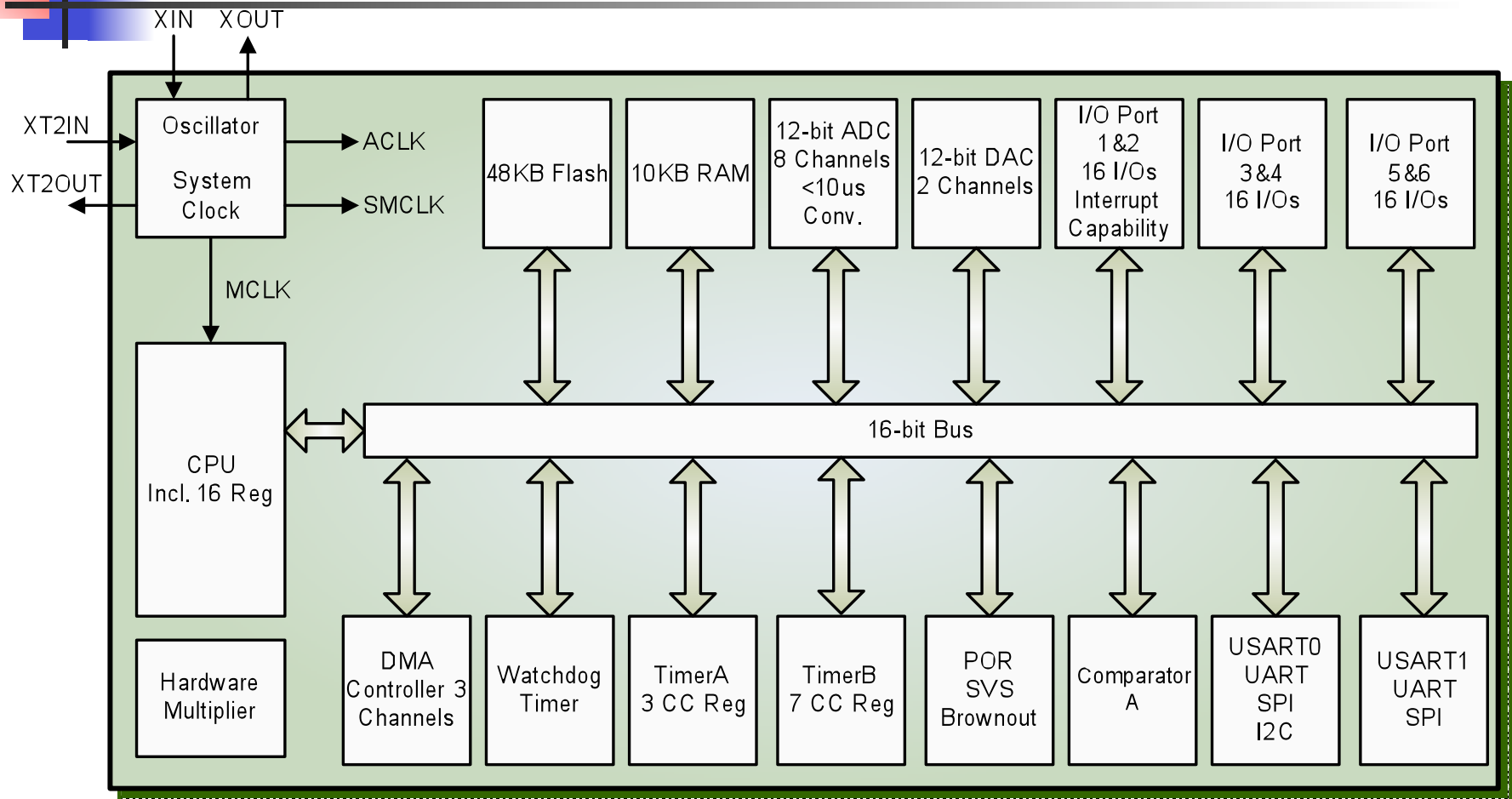




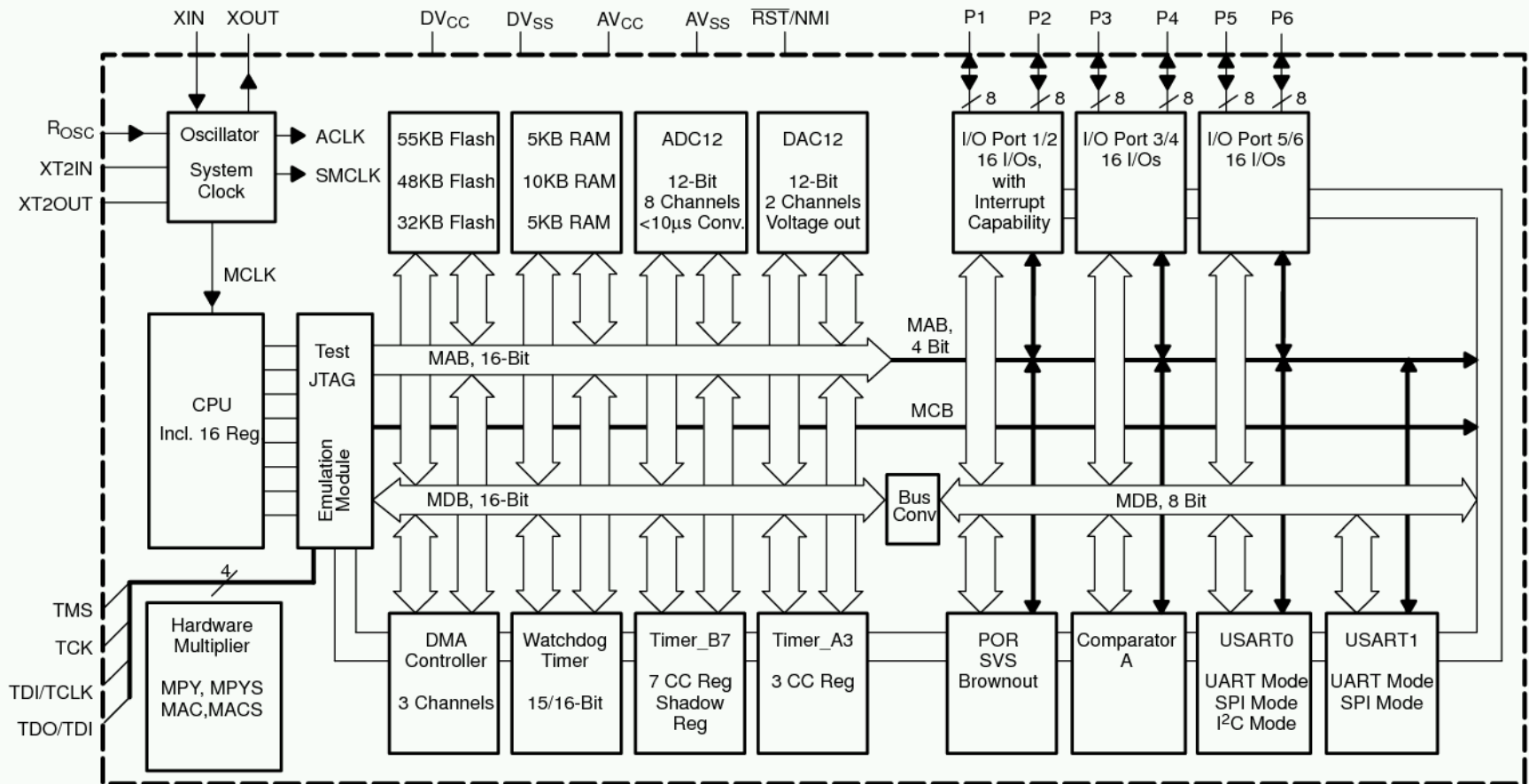
MSP430F1611



MSP430F1611 Function Block Diagram

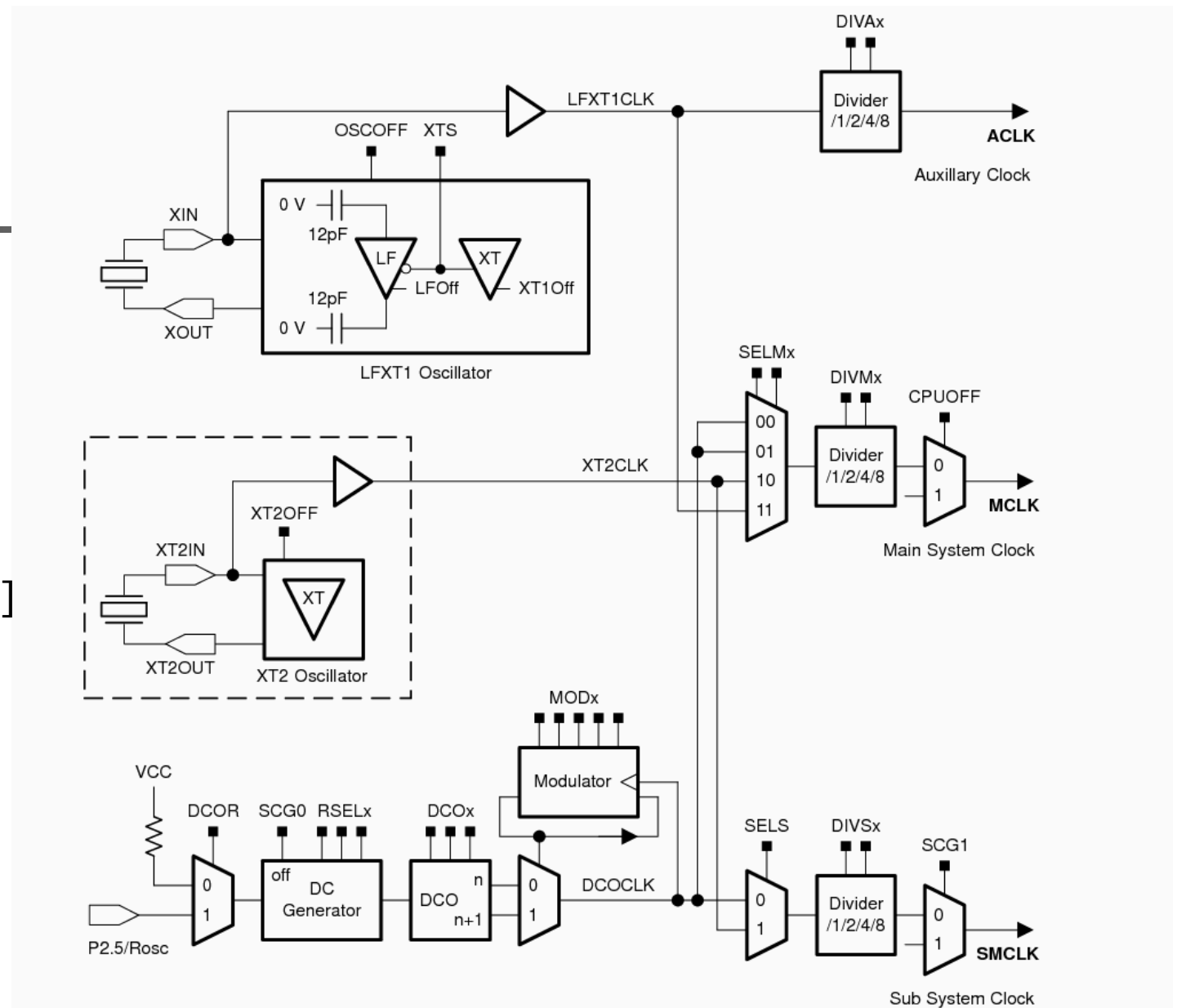


MSP430x161x



Clocks

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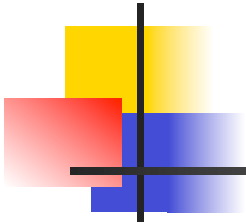


Table 4–1. Basic Clock Module Registers

Register	Short Form	Register Type	Address	Initial State
DCO control register	DCOCTL	Read/write	056h	060h with PUC
Basic clock system control 1	BCSCTL1	Read/write	057h	084h with PUC
Basic clock system control 2	BCSCTL2	Read/write	058h	Reset with POR
SFR interrupt enable register 1	IE1	Read/write	000h	Reset with PUC
SFR interrupt flag register 1	IFG1	Read/write	002h	Reset with PUC

Timer B

[pages: 73-, Chap. 12]

