More motivation for model checking

- ISSTA 1998 (March), Model Checking Without a Model:An Analysis of the Heart-Beat Monitor of a Telephone Switch using VeriSoft, by 3 researchers from Lucent and Bell Labs.

Abstract

- VeriSoft a tool for systematically exploring state spaces of systems composed of several concurrent processes written in full-fledged programing languages.
- State space: directed graph represents combined behavior of concurrent components.
- VeriSoft detects coordination problems. Executes thousands of tests per minute.

Abstract

- Application to be tested: Heart-Beat Monitor (HBM) of a telephone switch. Used for faster routing of data.
- Discuss steps of analysis of HBM.
- No modeling was necessary: only a few hours up to tests instead of several days or weeks.

Introduction

- Systematic state exploration, e.g. temporal-logic model-checking, attracting growing attention.
- Existing tools restricted to explore the state space of an abstract description of the system.