

John Willis O'Leary

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Education

Ph.D., Electrical Engineering, Cornell University, Ithaca, NY, 1995. Dissertation: *A Model and Proof Technique for Verifying Hardware Compilers for Communicating Processes.*

M.Eng., Systems and Computer Engineering, Carleton University, Ottawa, Canada, 1989. Thesis: *A VLSI Architecture for Linear Predictive Analysis of Speech.*

B.Sc., Electrical Engineering, The University of Calgary, Calgary, Canada, 1985.

Positions

April-June 2015 Oliver Smithies Visiting Lecturership, Trinity Term, Balliol College, University of Oxford

2010-present Principal Engineer; Formal Verification Center of Expertise, Intel

2002-2010 Principal Engineer and Manager, Logic Verification; Strategic CAD Labs, Intel Corporation

1995-2002 Senior Engineer, Staff Engineer, Senior Staff Engineer; Strategic CAD Labs, Intel Corporation

1990-1995 Research assistant; School of Electrical Engineering, Cornell University

1987-1990 Member of Scientific Staff; Bell-Northern Research, Ltd. Ottawa, Canada

1985-1987 Research assistant; Department of Systems and Computer Engineering, Carleton University

Professional Service

Panelist, National Science Foundation, 2014.

Chair, Verification subcommittee, *ACM/IEEE Design Automation Conference*, 2012-2014.

Co-chair, *Workshop on Hardware Design and Functional Languages (HFL09)*, York, UK, March 2009.

Co-chair, *Workshop on Multithreading in Hardware and Software: Formal Approaches to Design and Verification (TV06)*, Seattle, WA, August 21-22, 2006.

Program co-chair, *Third ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'05)*, Verona, Italy, July 2005.

General chair, *Fourth International Symposium on Formal Methods in Computer-Aided Design (FMCAD'02)*, Portland, OR, 6-8 November 2002.

Steering committee member, *Formal Methods in Computer-Aided Design* conference series. 2002-2006.

Industrial liaison, representing Intel Corporation in the Semiconductor Research Consortium (SRC) from 2000-2010. Contributor to research needs documents for SRC.

Technical program committee membership:

- *16th International Conference on Formal Methods in Computer-Aided Design (FMCAD'16)*. California, October 2016.
- *Design, Automation and Test in Europe (DATE'16)*. Dresden, Germany, March 2016.
- *13th International Workshop on the ACL2 Theorem Prover and Its Applications*. Austin, TX, October 2015.
- *13th ACM-IEEE International Conference on Formal Methods and Models for System Design*. Austin, TX. September 2015.
- *Twelfth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'14)*. Lausanne, Switzerland, October 2014.
- *Thirteenth International Symposium on Formal Methods in Computer-Aided Design*, Portland, OR, October 2013.
- *Twelfth International Symposium on Formal Methods in Computer-Aided Design*, Cambridge, UK, October 2012.
- *Tenth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'12)*. Arlington, VA, July 2012.
- *Ninth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'11)*. Cambridge, UK, July 2011.
- *48th Design Automation Conference (DAC'11)*. San Diego, CA. June 2011.
- *Tenth International Symposium on Formal Methods in Computer-Aided Design*, Lugano, Switzerland, October 2010.

- *Seventh ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'09)*, Cambridge, MA, July 13-15, 2009.
- *Eighth International Symposium on Formal Methods in Computer-Aided Design*, Portland, OR, November 2008.
- *Sixth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'08)*, Anaheim, CA, June 5-7, 2008.
- *Seventh International Workshop on Designing Correct Circuits*, Budapest, Hungary, April 2008.
- *Seventh International Symposium on Formal Methods in Computer-Aided Design*, Austin, TX, November 2007.
- *Fifth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'07)*, Nice, France, May 30-June 1, 2007.
- *Sixth International Symposium on Formal Methods in Computer-Aided Design*, San Jose, CA, November 12-16, 2006
- *Fourth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'06)*, Napa Valley, California, July 27-29, 2006.
- *Sixth International Workshop on Designing Correct Circuits*, Vienna, Austria, April 2006
- *13th Advanced Research Working Conference on Correct Hardware Design and Verification Methods*, Saarbrucken, Germany, October 2005
- *17th Conference on Computer Aided Verification*, Edinburgh, Scotland, July 2005
- *Fifth International Symposium on Formal Methods in Computer-Aided Design*, Austin, TX, November 2004
- *Fifth International Workshop on Designing Correct Circuits*, Barcelona, Spain, April 2004
- *12th Advanced Research Working Conference on Correct Hardware Design and Verification Methods*, L'Aquila, Italy, October 2003
- *Fourth International Symposium on Formal Methods in Computer-Aided Design*, Portland, OR, November 2002
- *Fourth International Workshop on Designing Correct Circuits*, Grenoble, France, April 2002
- *11th Advanced Research Working Conference on Correct Hardware Design and Verification Methods*, Livingston, Scotland, September 2001
- *Third International Symposium on Formal Methods in Computer-Aided Design*, Austin, TX, November 2000

Dissertation and Thesis Committees:

- Ariel Cohen, *Verification of Transactional Memories and Recursive Programs*, Ph.D., New York University, 2008.
- Christian Tabone, *Meta-Functional Languages for Hardware Design*, M.Sc., University of Malta, 2009.
- Cherif Salama, *Static Analysis for Circuit Families*, Ph.D., Rice University, 2010.
- Krishnaji Desai, *Symbolic asynchronous hardware protocol verification for compositions with relative timing*, M.S., University of Utah, 2010.

Publications

Edited books

C. Heitmeyer and J.W. O’Leary (eds.), *Formal Methods and Models for Co-Design: 3rd ACM & IEEE International Conference: Proceedings*, IEEE Computer Society (2005). ISBN 0-7803-9227-2.

M.D. Aagaard and J.W. O’Leary (eds.), *Formal Methods in Computer-Aided Design: 4th International Conference: Proceedings*, Lecture Notes in Computer Science, vol. 2517 (Springer-Verlag, 2002). ISSN 0302-9743.

Edited journals

G. Gopalakrishnan and J. O’Leary (eds.), Special issue on Proceedings of the Thread Verification Workshop (TV 2006), *Electronic Letters in Theoretical Computer Science*, vol. 174, no. 9 (June 2007), pp. 1-166.

Journal and magazine articles

C. Salama, G. Malecha, W. Taha, J. Grundy and J. O’Leary, “Static Consistency Checking for Verilog Wire Interconnects: Using Dependent Types to Check the Sanity of Verilog Descriptions”, *Higher Order and Symbolic Computing*, vol 24, no. 1-2 (June 2011), pp. 81-114.

J. Gillenwater, G. Malechi, C. Salama, A. Zhu, W. Taha, J. Grundy and J. O’Leary, “Synthesizable High Level Hardware Descriptions”, *New Generation Computing*, vol. 28, no. 4 (December 2010), pp. 339-369.

S. Krstic, R.B. Jones, and J.W. O’Leary, “Mothers of Pipelines”, *Electronic Letters in Theoretical Computer Science*, vol. 174, no. 8 (November 2006), pp. 7-22.

J. Grundy, T.F. Melham, and J.W. O’Leary, “A Reflective Functional Language for Hardware Design and Theorem Proving”, *Journal of Functional Programming*, vol. 16, no. 2 (March 2006).

C.-J.H. Seger, R.B. Jones, J.W. O’Leary, T. Melham, M.D. Aagaard, C. Barrett, and D. Syme, “An Industrially Effective Environment for Formal Hardware Verification”, *IEEE Transactions on Computer-Aided Design*, vol. 24, no.9 (September 2005), pp. 1381-1406.

R. B. Jones, J.W. O’Leary, C.-J. H. Seger, M. D. Aagaard, and T. F. Melham, “Practical Formal Verification in Microprocessor Design”, *IEEE Design & Test of Computers*, vol. 18, no. 4 (July/August 2001), pp. 16–25.

J.W. O’Leary, X. Zhao, R. Gerth, and C.-J.H. Seger, “Formally Verifying IEEE Compliance of Floating-Point Hardware”, *Intel Technology Journal* (First Quarter, 1999).

J.W. O’Leary, G.M. Brown, and W. Luk, “Verified Compilation of Communicating Processes into Clocked Circuits”, *Formal Aspects of Computing*, vol. 9 (1998), pp. 537-559.

J.W. O’Leary and G.M. Brown, “Synchronous Emulation of Asynchronous Circuits”, *IEEE Transactions on Computer-Aided Design*, vol. 16, no. 2 (February 1997), pp. 205-209.

G.M. Brown, W. Luk, and J.W. O’Leary, “Retargeting a Hardware Compiler using Protocol Converters”, *Formal Aspects of Computing*, vol. 8, no. 2 (1996), pp. 209-237.

A.S. Wenban, J.W. O’Leary, and G.M. Brown, “Codesign of Communication Protocols”, *Computer*, vol. 26, no.12 (December 1993), pp. 46-52.

Refereed conference papers

J. O’Leary and D. Russinoff, “Modeling Algorithms in SystemC and ACL2”. *Twelfth International Workshop on the ACL2 Theorem Prover and its Applications*. Vienna, July 2014.

J. O’Leary, R. Kaivola and T. Melham, “Relational STE and Theorem Proving for Formal Verification of Industrial Circuit Designs”. *Formal Methods in Computer-Aided Design: Thirteenth International Conference, FMCAD 2013*: Portland, October 2013.

K. Desai, K.S. Stevens, and J. O’Leary, “Symbolic Verification of Timed Asynchronous Hardware Protocols”. *IEEE Annual Symposium on VLSI (ISVLSI 2013)*. Brazil, August 2013.

B.A. Brady, R.E. Bryant, S.A. Seshia, and J.W. O’Leary, “ATLAS: Automatic Term-level abstraction of RTL designs”, *Eighth ACM-IEEE International Conference on Formal Methods and Models for Codesign*, Grenoble, July 2010.

J. O’Leary, M. Talupur, and M. Tuttle, “Protocol Verification using Flows: An Industrial Experience”, *Formal Methods in Computer-Aided Design: Ninth International Conference, FMCAD 2009*: Austin, November 2009.

J. O’Leary, B. Saha, and M.R. Tuttle, “Model Checking Transactional Memory with Spin”, *Proc. of the 29th International Conference on Distributed Computing Systems (ICDCS 2009)*. June 2009.

C. Salama, G. Malecha, W. Taha, J. Grundy and J. O’Leary, “Static Consistency Checking for Verilog Wire Interconnects: Using Dependent Types to Check the Sanity of

Verilog Descriptions”, *ACM SIGPLAN Workshop on Partial Evaluation and Program Manipulation (PEPM)*, January 2009.

John O’Leary, Bratin Saha and Mark R. Tuttle, “Brief Announcement: Model Checking Transactional Memory with Spin”, *Proc. Of the 27th ACM Symposium on Principles of Distributed Computing (PODC’08)*, August 2008.

David James, Tim Leonard, John O’Leary, Murali Talupur and Mark R. Tuttle, “Brief Announcement: Extracting Models from Design Documents with Mapster”, *Proc. Of the 27th ACM Symposium on Principles of Distributed Computing (PODC’08)*, August 2008.

J. Gillenwater, G. Malecha, C. Salama, A. Zhu, W. Taha, J. Grundy and J. O’Leary, “Statically Guaranteeing Synthesizability of High Level Hardware Descriptions”, *ACM SIGPLAN Workshop on Partial Evaluation and Program Manipulation (PEPM)*, January 2008.

A. Cohen, J. O’Leary, A. Pnueli, M. Tuttle, and L. Zuck, “Verifying Correctness of Transactional Memories”, *Formal Methods in Computer-Aided Design: Seventh International Conference, FMCAD 2007: Austin*, November 2007.

S. Krstic, J. Cortadella, M. Kishinevsky, and J.W. O’Leary, “Synchronous Elastic Networks”, *Formal Methods in Computer-Aided Design: Sixth International Conference, FMCAD 2006: San Jose*, November 2006.

M. Kishinevsky, J. Cortadella, B. Grundmann, S. Krstic, and J. O’Leary, “Synchronous Elastic Circuits”, *Computer Science - Theory and Applications, First International Computer Science Symposium in Russia, (CSR) 2006: St. Petersburg, Russia*, May 2006.

J. O’Leary and M. Roncken, “Rob Tristan Gerth: 1956-2003”, *Computer Aided Verification, 16th International Conference, (CAV) 2004: Boston*, July 13-17, 2004.

M. D. Aagaard, R. B. Jones, T. F. Melham, J. W. O’Leary, and C.-J. H. Seger, “A Methodology for Large-Scale Hardware Verification”, in *Formal Methods in Computer-Aided Design: Third International Conference, FMCAD 2000: Austin, November 2000: Proceedings*, edited by W. A. Hunt, Jr. and S. D. Johnson, Lecture Notes in Computer Science, vol. 1954 (Springer-Verlag, 2000), pp. 263–282.

M. D. Aagaard, T. F. Melham, and J. W. O’Leary, “Xs are for Trajectory Evaluation, Booleans are for Theorem Proving”, in *Correct Hardware Design and Verification Methods: 10th IFIP WG10.5 Advanced Research Working Conference: Bad Herrenalb, September 1999: Proceedings*, edited by L. Pierre and T. Kropf, Lecture Notes in Computer Science, vol. 1703 (Springer-Verlag, 1999), pp. 202–218.

P.-H. Ho, Y. Hoskote, T. Kam, M. Khaira, J. O’Leary, X. Zhao, Y.-A. Chen, and E. Clarke, “Verification of a Complete Floating-Point Unit using Word-Level Model Checking”, in *Formal Methods in Computer-Aided Design: First International*

Conference, FMCAD '96: Palo Alto, CA, USA, November 1996: Proceedings, Lecture Notes in Computer Science, vol. 1166 (Springer-Verlag, 1996), pp.19-33.

J. He, G.M. Brown, W. Luk, and J.W. O'Leary, "Deriving Handshake Modules for a Multi-target Hardware Compiler", *3rd Workshop on Designing Correct Circuits*, edited by M. Sheeran and S. Singh, Electronic Workshops in Computing (Springer-Verlag, 1996).

A.S. Wenban, G.M. Brown, and J.W. O'Leary, "Developing Interface Libraries for Reconfigurable Data Acquisition Boards", *Field-Programmable Logic and Applications*, edited by W. Luk and W. Moore, Lecture Notes in Computer Science, vol. 975 (Springer-Verlag, 1996), pp. 331-340.

M. Leeser and J.W. O'Leary, "Verification of a Subtractive Radix-2 Square Root Algorithm and Implementation", *International Conference on Computer Design*, (Institute of Electrical and Electronics Engineers, 1995), pp. 526-531.

J.W. O'Leary, M. Leeser, J. Hickey, and M. Aagaard, "Non-restoring Integer Square Root: A Case Study in Design by Principled Optimization", *Theorem Provers in Circuit Design: Theory, Practice and Experience*, edited by R. Kumar and T. Kropf, Lecture Notes in Computer Science, vol. 901 (Springer-Verlag, 1995), pp. 52-71.

G.M. Brown, W. Luk, and J.W. O'Leary, "Retargeting a Hardware Compiler Proof using Protocol Converters", *First International Symposium on Advanced Research in Asynchronous Circuits and Systems* (Institute of Electrical and Electronics Engineers, November 1994), pp. 54-63.

J.W. O'Leary, M. Linderman, M. Leeser, and M. Aagaard, "HML: A Hardware Description Language based on SML", *Computer Hardware Description Languages and their Applications*, edited by D. Agnew, L. Claesen and R. Camposano, IFIP Transactions A-32 (Elsevier, North-Holland, 1993), pp. 327-334.

A.S. Wenban, J.W. O'Leary, and G.M. Brown, "Codesign of Communication Protocols", *Proceedings of the First International Workshop on Hardware/Software Codesign*, October 1992.

J.W. O'Leary, D.D. Falconer, and C.H. Chan, "A VLSI Architecture for Linear Predictive Analysis of Speech", *Canadian Conference on Very Large Scale Integration*, Winnipeg, MB, 1987.

Invited talks, panels, and workshops (unrefereed or lightly refereed)

J. Gillenwater, G. Malecha, C. Salama, A. Y. Zhu, W. Taha, J. Grundy and J. O'Leary, "Formalizing and Enhancing Verilog", *SRC TECHCON*, 2007, Austin, TX, USA

C. Andraos, J. Gillenwater, G. Malecha, A. Y. Zhu, W. Taha, J. Grundy and J. O'Leary, "Synthesizable Verilog", *Workshop on Hardware Design and Functional Languages (HFL)*, 2007, Braga, Portugal.

S. Krstic, R.B. Jones, and J.W. O'Leary, "Mothers of Pipelines", *Fourth Workshop on Pragmatics of Decision Procedures in Automated Reasoning*, Seattle, WA, August 2006.

T.F. Melham and J.W. O'Leary, "A functional HDL for reFLect", *Sixth Workshop on Designing Correct Circuits*, Vienna, Austria, March 2006.

S. Krstic, M. Kishinevsky, J. Cortadella and J. O'Leary, "Networks of elastic circuits", *Sixth Workshop on Designing Correct Circuits*, Vienna, Austria, March 2006.

J.W. O'Leary, "Using a reflective functional language for hardware verification and theorem proving", INRIA Rocquencourt, March 2006.

J.W. O'Leary, "Using a reflective functional language for hardware verification and theorem proving", Indiana University Informatics Colloquium, 2005.

J.W. O'Leary, "Using a reflective functional language for hardware verification and theorem proving", *APPSEM'05*, Germany, September 2005.

Panelist: "Design for Verification", *3rd ACM/IEEE Conference on Formal Methods and Models for Codesign (MEMOCODE'05)*, Verona, Italy, 2005.

J.W. O'Leary, J. Grundy and T.F. Melham, "A Reflective Functional Language for Hardware Design and Theorem Proving", *IFIP WG 2.8 meeting*, November 2004.

J.W. O'Leary, "Formal Verification in Intel CPU Design", *2nd ACM/IEEE Conference on Formal Methods and Models for Codesign (MEMOCODE'04)*, San Diego, CA, June 2004.

J.W. O'Leary, J. Grundy and T.F. Melham, "A Reflective Functional Language for Hardware Design and Theorem Proving", *Fifth Workshop on Designing Correct Circuits*, Barcelona, Spain, March 2004.

Panelist, "Formal verification: prove it or pitch it", *40th ACM/IEEE Design Automation Conference*, Anaheim, CA, June 2003.

J.W. O'Leary, "Verification of Floating Point Hardware using Symbolic Trajectory Evaluation and Theorem Proving", *Microprocessor Test and Validation (MTV'03)*, Austin, TX, June 2003.

J.W. O'Leary and T.F. Melham, "A Stream-based Framework for Reasoning with STE and other LTL Verification Formalisms", *Fourth Workshop on Designing Correct Circuits*, Grenoble, France, April 2002.

J.W. O'Leary, "Using STE to Formally Verify Floating-point Hardware", *Workshop on Symbolic Trajectory Evaluation*, Chicago, June 2000.

J.W. O'Leary, "Formally verifying IEEE-compliance of floating-point hardware", Computer Science & Engineering Department, Oregon Graduate Institute, 1999.

J.W. O'Leary, "A model for verifying digital circuits", *Hardware Synthesis and Verification Workshop*, Cornell University, Ithaca, NY, August 14-16, 1996.

Dissertations

J.W. O'Leary, *A Model and Proof Technique for Verifying Hardware Compilers for Communicating Processes*, Ph.D. dissertation, School of Electrical Engineering, Cornell University, 1995.

J.W. O'Leary, *A VLSI Architecture for Linear Predictive Analysis of Speech*, M.Eng. thesis, Department of Systems and Computer Engineering, Carleton University, 1989.

Technical reports and other publications

J. Gillenwater, G. Malecha, C. Salama, A. Y. Zhu, W. Taha, J. Grundy, and J. O'Leary, "Synthesizable High Level Hardware Descriptions". Technical report, Rice University and Intel Strategic CAD Labs, <http://www.resourceaware.org/twiki/pub/RAP/VPP/FV-TR.pdf>, 2007

J. Grundy, T. Melham, and J.W. O'Leary, "A Reflective Functional Language for Hardware Design and Theorem Proving", Research Report RR-03-16, Computing Laboratory, University of Oxford (October 2003).

M. D. Aagaard, T. F. Melham, and J. W. O'Leary, "Xs are for Trajectory Evaluation, Booleans are for Theorem Proving (Extended Version)", Technical Report TR-2000-52, Department of Computing Science, University of Glasgow (January 2000).

J.W. O'Leary, "A Model for Verifying Digital Circuits", *Hardware Synthesis and Verification Workshop*, Cornell University, Ithaca, NY, August 14-16, 1996.

G.M. Brown, W. Luk, and John O'Leary, "Retargeting a Hardware Compiler Proof", Technical Report EE-CEG-94-10, School of Electrical Engineering, Cornell University, December 1994.

G.M. Brown, J.W. O'Leary, and A.S. Wenban, "Software/hardware codesign for reconfigurable systems", Technical Report EE-CEG-94-9, School of Electrical Engineering, Cornell University, October 1994.

A.S.. Wenban, J.W. O'Leary, and G.M. Brown, "Users' guide: Extended Promela Compiler, Hardware Promela Compiler, Hardware Promela Debugger, Codesign Front

End”, Technical Report EE-CEG-94-8, School of Electrical Engineering, Cornell University, October 1994.

J.W. O’Leary and G.M. Brown, “Synchronous Emulation of Asynchronous Circuits”, Technical Report EE-CEG-94-7, School of Electrical Engineering, Cornell University, November 1994.

G.M. Brown, W. Luk, and J.W. O’Leary, “Retargeting a hardware compiler using protocol converters”, Technical Report EE-CEG-94-1, School of Electrical Engineering, Cornell University, February 1994.

J.W. O’Leary, M. Linderman, M. Leeser, and M. Aagaard, “HML: A Hardware Description Language based on Standard ML”, Technical Report EE-CEG-92-7, School of Electrical Engineering, Cornell University, October 1992.

Citizenship

United States

Canada

Republic of Ireland